Claims

[c1] 1.A method for initializing a static random access memory (SRAM) device during power-up, the method comprising:
clamping one of a pair of bitlines of the SRAM device to a logic low potential while allowing the other of the pair of bitlines to be coupled to a charging logic high potential; and
forcing an SRAM storage cell within the SRAM device to a stable state by selectively allowing a wordline potential of a wordline associated with said SRAM storage cell to follow said charging logic high potential, thereby coupling said SRAM storage cell to said pair of bitlines.

[c2] 2.The method of claim 1, wherein said allowing said wordline potential to follow said charging logic high potential is implemented by selectively coupling a leakage current to said wordline, said leakage current originating from wordline driver circuitry associated with said wordline.

[c3] 3.The method of claim 2, wherein said clamping one of a pair of bitlines of the SRAM device to a logic low potential is implemented through activation of an NFET device

included within bitline precharging circuitry associated with said bitline pair.

[c4] 4.The method of claim 3, wherein said clamping one of a pair of bitlines of the SRAM device to a logic low potential and said coupling a leakage current to said wordline are gated by a power-on reset signal.

[c5] 5.The method of claim 3, wherein said power-on reset signal is generated on-chip.

[c6] 6.The method of claim 3, wherein said power-on reset signal is software controlled.

[c7] 7.The method of claim 2, wherein said leakage current is selectively coupled to said wordline through a NFET device configured to selectively isolate said wordline from ground potential.

[c8] 8.The method of claim 7, further comprising providing a separate leakage current source for said NFET device so as to prevent said NFET device from bleeding said leakage current originating from wordline driver circuitry away from said wordline.

[c9] 9.The method of claim 8, wherein said separate leakage current source comprises a PFET device.

[c10] 10.The method of claim 7, further comprising coupling

NFET devices within said SRAM cell to a p-well bias voltage above said logic low potential so as to reduce a threshold voltage thereof.

[c11] 11.An apparatus for initializing a static random access memory (SRAM) device during power-up, comprising:
a clamping device configured to hold one of a pair of bitlines of the SRAM device to a logic low potential while the other of the pair of bitlines is coupled to a charging logic high potential; and
an isolation device configured to force an SRAM storage cell within the SRAM device to a stable state by selectively allowing a wordline potential of a wordline associated with said SRAM storage cell to follow said charging logic high potential, thereby coupling said SRAM storage cell to said pair of bitlines.

[c12] 12.The apparatus of claim 11, wherein said isolation device is further configured to selectively couple a leakage current to said wordline, said leakage current originating from wordline driver circuitry associated with said wordline.

[c13] 13.The apparatus of claim 12, wherein said clamping device further comprises an NFET included within bitline precharging circuitry associated with said bitline pair.

[c14] 14.The apparatus of claim 13, wherein said clamping device and said isolation device are gated by a power-on reset signal.

[c15] 15.The apparatus of claim 13, wherein said power-on reset signal is generated on-chip.

[c16] 16.The apparatus of claim 13, wherein said power-on reset signal is software controlled.

[c17] 17.The apparatus of claim 12, wherein said isolation device further comprises an NFET configured to selectively isolate said wordline from ground potential.

[c18] 18.The apparatus of claim 17, further comprising a separate leakage current source for said isolation device so as to prevent said isolation device from bleeding said leakage current originating from wordline driver circuitry away from said wordline.

[c19] 19.The apparatus of claim 18, wherein said separate leakage current source comprises a PFET.

[c20] 20.The apparatus of claim 17, further comprising p-well bias voltage source for selectively coupling NFET devices within said SRAM cell to a p-well bias voltage above said logic low potential so as to reduce a threshold voltage thereof.